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| EXAMINER | |
|---|---|
| MCMAHON, DANIEL F | |

| ART UNIT | PAPER NUMBER |
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| 2117 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/591,193 | AZIMANE ET AL. | |
| | Examiner | Art Unit | |
| | DANIEL F. MCMAHON | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This action is in response to amendments filed May 19, 2009.

Claims 1, 9, and 17 have been amended.

Claims 1 – 24 are pending.

### *Response to Amendment*

1. The objection to the specification is withdrawn in light of the amendments to the claims.

### *Response to Arguments*

2. The objection to the drawing, under 37 C.F.R. 1.84(o) is withdrawn in light of applicant's argument.

3. Applicant's arguments, filed May 19, 2009 regarding the rejection of claims 1, 9, and 17, under 35 U.S.C. 112, first paragraph, have been fully considered but they are not persuasive.

Regarding applicant's argument, the examiner appreciates MPEP 608.01(o), specifically, that an applicant is not limited to the nomenclature used in the specification. Additionally, the examiner appreciates, as cited by the applicant, page 6, lines 22 – 26 and page 7, lines 6 – 9, that an external clock signal is provided during a test mode, and that the external clock signal may have a duty cycle lower or higher then 50%.

However, the specification does not disclose the internal clock signal independent of the duty cycle of the external clock. As cited in the specification, the external clock signal may have a duty cycle of lower or higher then 50% duty cycle (page 6, lines 22 – 26). However, the specification is silent as to any modification of the duty cycle of the internal clock signal; which would allow the duty cycle to differ from that of the external clock signal. As noted in paragraph 8, “There is a clock monitor for receiving an external clock signal and for providing an internal clock signal in dependence thereupon to the internal memory block.” As currently understood, the specification does not disclose a modification of the duty cycle of the internal clock signal, which is dependant on the external clock signal. As a result, the duty cycle of the internal clock signal with be the duty cycle of the external clock signal, which may be higher or lower then 50%. Further shown in figure 2, though elements CL, 152, and input 104.

4. Applicant's arguments, filed May 19, 2009 regarding the rejection of claim 2 – 4, under 35 U.S.C. 112, second paragraph, have been fully considered but they are not persuasive.

5. Regarding claim 2, applicant’s argument: the claim language is not ambiguous, in light of the specification, is not persuasive. The examiner continues to have difficulty grammatically parsing the limitation of the claim. The language "further comprising switching provision of the external clock signal received during the test mode to different

internal memory block" is ambiguous. In light of the specification, the examiner is still unclear if the applicant intends the external clock signal to have provisions which are switched to different internal memory blocks, or the external clock signal is switched though the use of a provision to the internal memory blocks. Additionally, the examiner is unclear as to what is received during the test mode, the external clock signal, as a single bit periodic signal, or some provision of the external clock signal which differs from the external clock signal.

6. Regarding claims 3 and 4, applicant's argument: the claim language is not ambiguous, in light of the specification, is not persuasive. Examiner maintains one of ordinary skill in the art would understand a "duty cycle" to be a property of a periodic signal, and not of a memory block. Applicant has not defined "duty cycle" with a broader scope then would be understood by one of ordinary skill in the art.

7. Applicant's arguments with respect to claim 1 - 24 have been considered but are moot in view of the new ground(s) of rejection.

## *Claim Rejections - 35 USC § 112 (old)*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 9, and 17 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amended limitation “wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal” is not supported by the specification filed August 30, 2006. Applicant is unpersuasive in the citation of page 4, lines 12 – 22. Page 4, lines 12 – 22 discloses an “external control... using the test system" and "the test system implemented for modifying the duty cycle". The cited specification does not disclose the modification of duty cycle of the internal clock signal independent of the duty cycle of the external clock signal. The specification discloses a test system that has the ability to control the duty cycle of the internal clock signal though the modification of the duty cycle of the external clock system, though the functionality of the external controls. Examiner understands that any manipulation of duty cycle for the internal clock signal and external clock signal is performed by the test system, external to the device under test.

For purposes of examination the examiner assumes that during a test mode the self-timed memory is powered by an external clock signal.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2 – 4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Regarding claim 2, the language "further providing switching provision" is ambiguous and fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Examiner is unclear if the intended meaning is "a switching provision" or "switching a provision".

6. Regarding claims 3 and 4, the language "duty cycle of the internal memory block" is ambiguous. One of ordinarily skill in the art would understand "duty cycle" to be a characteristic of a signal with a periodic or repetitive nature. It is unclear how applicant intends the internal memory block to have a duty cycle. The claim therefor fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

***Prior Art Rejections***

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

***Claim Rejections - 35 USC § 103 (New)***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 – 13, 16 – 20, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill et al. U.S. Patent 6,115,836 (herein Churchill), in view of Irrinki et al. U.S. Patent 5,822,228 (herein Irrinki) and Savir U.S. Patent 5,642,362 (herein Savir).

9. Regarding claim 1, Churchill teaches: A method for providing an external clock signal (figure 2, clk) to an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218) of a self-timed memory (figure 2, element 200), the method comprising: receiving an internal clock signal (figure 9, element 916) from a clock monitor of the self-timed memory (figure 9, element 902; figure 11c, element 1102); receiving an external clock signal (figure 2, clk); receiving a control signal (figure 9, element 912); and providing, in dependence upon the control signal, the internal clock signal to the internal memory block during a normal mode of operation of the self-timed memory (column 18,

lines 6 – 12), and the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10). Churchill does not explicitly teach: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal; and detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory.

Irrinki teaches: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal (column 4, lines 13 – 15; claim 2).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill: a method for providing an external clock signal to an internal memory block of a self-timed memory comprising receiving an internal clock signal and receiving an external clock signal with the teaching of Irrinki: an external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal for the purpose of performing propagation delay measurements (column 3, lines 39 – 46). Propagation delay testing is well known in the art (column 3, lines 39 – 46). Modification of the duty cycle of an external clock signal is well known in art for the purpose of propagation delay testing (column 4, lines 10 – 24). One of ordinary skill in the art, at the time of the invention, would have recognized that applying the known technique to the known device would have yielded a predictable result.

Savir teaches: detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory (column 1, lines 10 – 30).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill: a method for providing an external clock signal to an internal memory block of a self-timed memory comprising receiving an internal clock signal and receiving an external clock signal with the teaching of Savir: detecting a slow-to-rise delay or a slow-to-fall delay for the purpose of device testing (column 1, lines 10 – 36). Slow-to-rise (STR) and slow-to-fall (STF) fault testing is well known technique in the art. One of ordinary skill in the art, at the time of the invention, would have recognized that applying the known technique to the known device would have yielded a predictable result.

10. Regarding claim 2, Churchill additionally teaches: switching provision of the external clock signal received during test mode to different internal memory blocks according to a predetermined test pattern (column 18, lines 46 – 48; column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

11. Regarding claim 3, Churchill teaches the limitations of the parent claim, claim 2. Churchill additionally teaches: the delay circuit programmed for generating an internal clock with a duty cycle less then 50% (column 17, lines 33 – 50). Churchill additionally teaches: an external clock with a configurable duty cycle (column 19, lines 5 – 10). Churchill does not explicitly teach: the duty cycle of the external clock signal received

during test mode comprising a duty cycle lower than a 50% duty cycle of the internal memory block.

Irrinki teaches: the duty cycle of the external clock signal received during test mode comprising a duty cycle lower than a 50% duty cycle of the internal memory block (column 3, lines 39 – 46). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

12. Regarding claim 4, Churchill additionally teaches: the duty cycle of the external clock signal received during test mode comprises a duty cycle higher than a 50% duty cycle of the internal memory block (column 18, lines 46 – 48; column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

13. Regarding claim 5, Churchill additionally teaches: providing internal clock signal to the internal memory block in an absence of the control signal (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

14. Regarding claim 6, Churchill additionally teaches: receiving a control signal indicating initiation of the test mode (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

15. Regarding claim 7, Churchill additionally teaches: receiving a control signal indicating termination of the test mode (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

16. Regarding claim 8, Churchill additionally teaches: receiving the control signal during the test mode (column 19, lines 5 – 10). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

17. Regarding claim 9, Churchill teaches: A self-timed memory (figure 2) comprising: an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a clock monitor (figure 9, 902) for receiving an external clock signal (figure 2, clk) and for providing a clock signal (figure 9, element 902) to the internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a test system (figure 9, element 908, 910) interposed between the clock monitor (figure 9, 902) and the internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218). The test system comprising: an internal clock signal input port (figure 9, element 908) in signal communication with the clock monitor for receiving an internal clock signal (figure 9, element 916); an external clock signal input port (figure 9, element 910) for receiving the external clock signal (figure 9, element 914); a control signal input port (figure 9, element 908) for receiving a control signal (figure 9, element 912); an output port in signal communication with the internal memory block (figure 2, element 222); and a multiplexer in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port, and the output port (figure 9, element 908, 910);

wherein the multiplexer is configured to receive the internal clock signal, the external clock signal, and the control signal; and wherein the multiplexer is further configured to provide, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10). Churchill does not explicitly teach: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal; and detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory.

Irrinki teaches: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal (column 4, lines 13 – 15; claim 2).

Savir teaches: detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory (column 1, lines 10 – 30). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

18. Regarding claim 10, Churchill additionally teaches: the clock monitor comprises an input port for receiving the external clock signal (figure 9, element 902, signal 914) and wherein the input port is connected to the external clock signal input port of the test system (figure 9, element 908. 910, signal 914). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

19. Regarding claim 11, Churchill additionally teaches: test circuitry in signal communication with the test system (figure 2, element 212), the test circuitry for providing the control signal to the test system and for providing the external clock signal to the test system during the test mode (column 5, lines 13 – 25).

20. Regarding claim 12, Churchill additionally teaches: the internal memory block comprises an address decoder (figure 2, element 204, 208). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

21. Regarding claim 13, Churchill additionally teaches: the internal memory block comprises a sense amplifier (figure 2, element 214). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

22. Regarding claim 16, Churchill additionally teaches: the internal memory block comprises input/output latches (figure 2, element 216, 218). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

23. Regarding claim 17, Churchill teaches: A self-timed memory (figure 2) comprising: an internal memory block (figure 2, element 202, 204, 206, 208, 214, 216, 218); a clock monitor (figure 9, 902) for receiving an external clock signal (figure 2, clk) and for providing a clock signal (figure 9, element 902) to the internal memory block

(figure 2, element 202, 204, 206, 208, 214, 216, 218); a test system (figure 9, element 908, 910) interposed between the clock monitor (figure 9, 902) and the internal memory block(figure 2, element 202, 204, 206, 208, 214, 216, 218). The test system comprising: an internal clock signal input port (figure 9, element 908) in signal communication with the clock monitor for receiving an internal clock signal (figure 9, element 916); an external clock signal input port (figure 9, element 910) for receiving the external clock signal (figure 9, element 914); a control signal input port (figure 9, element 908) for receiving a control signal (figure 9, element 912); an output port in signal communication with the internal memory block (figure 2, element 222); and control circuitry in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port and the output port (figure 9, element 908, 910); wherein the control circuitry is configured to receive the internal clock signal, the external clock signal, and the control signal; and wherein the control circuitry is further configured to provide, in dependence upon the control signal, the internal clock signal via the output port to the internal memory block during a normal mode of operation of the self-timed memory (column 18, lines 6 – 12), and for providing the external clock signal to the internal memory block during a test mode of the self-timed memory (column 19, lines 5 – 10). Churchill does not explicitly teach: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal; and detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory..

Irrinki teaches: wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal (column 4, lines 13 – 15; claim 2).

Savir teaches: detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test mode of the self-timed memory (column 1, lines 10 – 30). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

24. Regarding claim 18, Churchill additionally teaches: the control circuitry comprises a multiplexer (figure 9, element 908, 910). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

25. Regarding claim 19, Churchill additionally teaches: the internal memory block comprises an address decoder (figure 2, element 204, 208). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

26. Regarding claim 20, Churchill additionally teaches: the internal memory block comprises a sense amplifier (figure 2, element 214). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

27. Regarding claim 23, Churchill additionally teaches: the internal memory block comprises input/output latches (figure 2, element 216, 218). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

28. Regarding claim 24, Churchill additionally teaches: test circuitry in signal communication with the test system (figure 2, element 212), the test circuitry for providing the control signal to the test system and for providing the external clock signal to the test system during the test mode (column 5, lines 13 – 25). And in view of the motivation previously stated above, for claim 1, the claim is rejected.

29. Claims 14, 15, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Churchill and Irrinki, in view of Choi, U.S. Patent 6,324,115 (herein Choi).

30. Regarding claim 14, Churchill and Irrinki teach the limitations of the parent claim, claim 9. Churchill additionally teaches: the internal memory block comprising a column decoder (figure 2, 208). Churchill does not explicitly teach: the internal memory block comprising a bank decoder.

Choi teaches: an internal memory block comprising a bank decoder (figure 1, element 160).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an

internal memory block, and a column decoder, as cited above, with the teaching of Choi, a bank decoder, for the purpose of addressing memory (column 1, lines 19 – 27). A self-timed memory is a well known device in the art. A bank decoder for addressing internal memory blocks is a well known technique (column 1, lines 38 – 41). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded the predictable result of addressable memory (abstract).

31. Regarding claim 15, Churchill and Irrinki teach the limitations of the parent claim, claim 9. Churchill teaches the limitations of the parent claim, claim 9. Churchill does not explicitly teach: t the predictable result of addressable memory (abstract). he internal memory block comprising a precharge and discharge circuitry.

Choi teaches: the internal memory block comprising a precharge and discharge circuitry (figure 1, element 310, 320).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, as cited above, with the teaching of Choi, precharge and discharge circuitry. A self-timed memory is a well known device in the art. Precharge and discharge circuitry for accessing internal memory blocks is a well known technique (column 2, lines 51 – 58). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable the predictable result of addressable memory (abstract).

32. Regarding claim 21, Churchill and Irrinki teach the limitations of the parent claim, claim 20. Churchill additionally teaches: the internal memory block comprising a column decoder (figure 2, 208). Churchill does not explicitly teach: the internal memory block comprising a bank decoder.

Choi teaches: an internal memory block comprising a bank decoder (figure 1, element 160).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, and a column decoder, as cited above, with the teaching of Choi; a bank decoder, for the purpose of addressing memory (column 1, lines 19 – 27). A self-timed memory is a well known device in the art. A bank decoder for addressing internal memory blocks is a well known technique (column 1, lines 38 – 41). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable the predictable result of addressable memory (abstract).

33. Regarding claim 22, Churchill and Irrinki teach the limitations of the parent claim, claim 21. Churchill teaches the limitations of the parent claim, claim 9. Churchill does not explicitly teach: the internal memory block comprising a precharge and discharge circuitry.

Choi teaches: the internal memory block comprising a precharge and discharge circuitry (figure 1, element 310, 320).

A person of ordinary skill in the art, at the time of the invention, would find it obvious to combine the teachings of Churchill, a self-timed memory comprising an internal memory block, as cited above, with the teaching of Choi; precharge and discharge circuitry. A self-timed memory is a well known device in the art. Precharge and discharge circuitry for accessing internal memory blocks is a well known technique (column 2, lines 51 – 58). One of ordinary skill in the art, at the time of the invention would have recognized that applying the known technique to the known device would have yielded predictable the predictable result of addressable memory (abstract).

## ***Conclusion***

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL F. MCMAHON whose telephone number is (571)270-3232. The examiner can normally be reached on M-Th 8am-5pm(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dfm
08/12/2009

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117